REMARKS

Applicants respectfully request reconsideration of this application. Claims 1-22 are pending. No claims have been canceled or added. Claims 1, 8, 11, and 18 have been amended.

Claim 11 was objected to because of minor informalities. Accordingly, Applicants have amended claim 11 to remove the informalities. Withdrawal of the objection is respectfully requested.

Claims 15-17 were rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. Accordingly, Applicants have amended the definition of "machine-accessible medium" in paragraph [0018] on p. 6 of the specification to overcome the rejection. Withdrawal of the rejection is respectfully requested.

Claims 1-2, 4-5, 7-9, and 12-14 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Publication No. 2003/0005346 of Zumkehr ("Zumkehr"). Applicants respectfully traverse the rejection.

Claim 1 as amended recites:

> a plurality of input/output (I/O) buffers coupled to the plurality of DLLs to output the plurality of signals to one or more memory devices coupled to the memory interface after adjusting the timing.

(Claim 1 as amended; emphasis added)

In contrast, Zumkehr fails to disclose the above limitation. However, the Office Action analogized the splitter 310 in Zumkehr to be the I/O buffers as claimed. Applicants respectfully disagree with the analogy. The splitter 310 is for splitting an

input signal into two signals, namely one representative of the input signal and the other being an inverted representation of the input signal. Zumkehr does not disclose, suggest, or imply that the splitter 310 is an I/O buffer. As is commonly understood in the relevant art, a splitter is not an I/O buffer. Further, the splitter 310 is part of the slave strobe delay device 210, which is analogized to be the DLL as claimed. The splitter 310 is *not* coupled to the slave strobe delay device 210 because the splitter 310 is *part* of the slave strobe delay device 210. Moreover, the splitter 310 outputs the two signals to the associated latches 372 and 374 of the memory controller, not to the memory 50 coupled to the memory controller 40 (Zumkehr, para. [0023]; Figures 1 & 4). Therefore, the splitter 310 in Zumkehr is distinct and separate from the I/O buffers as claimed. For at least this reason, Zumkehr fails to anticipate claim 1 as amended. Withdrawal of the rejection is respectfully requested.

For the reason discussed above with respect to claim 1, claim 8 is not anticipated by Zumkehr. Withdrawal of the rejection is respectfully requested.

Claims 2, 4-5, 7, 9, and 12-14 depend, directly or indirectly, from claims 1 and 8 respectively. For at least the reason discussed above with respect to claims 1 and 8, claims 2, 4-5, 7, 9, and 12-14 are not anticipated by Zumkehr. Withdrawal of the rejection is respectfully requested.

Claims 3, 10-11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Zumkehr in view of Adkisson (US 2004/0225910). Applicants respectfully traverse the rejection.

Claim 3 depends from claim 1, and thus, includes every limitation set forth in claim 1. As discussed above, Zumkehr fails to disclose the limitation of a plurality of I/O buffers coupled to the plurality of DLLs to output the plurality of signals to one or more

memory devices coupled to the memory interface after adjusting the timing. Further, Adkisson fails to make up the deficiencies in Zumkehr. Adkisson discloses a controller arrangement for effectuating data transfer across a clock boundary between a core clock domain and a bus clock domain (Adkisson, abstract). Adkisson does not disclose a plurality of I/O buffers coupled to the plurality of DLLs to output the plurality of signals to one or more memory devices coupled to the memory interface after adjusting the timing. Since neither Zumkehr nor Adkisson, alone or in combination, discloses every limitation set forth in claim 3, claim 3 is patentable over Zumkehr in view of Adkisson. Withdrawal of the rejection is respectfully requested.

Claims 10-11 depend from claim 8, and thus include every limitation set forth in claim 8. For the reason discussed above with respect to claim 1, Zumkehr and Adkisson, alone or in combination, do not disclose every limitation set forth in claim 8. Thus, claims 10-11 are patentable over Zumkehr in view of Adkisson. Withdrawal of the rejection is respectfully requested.

Claim 6 is rejected under 35 U.S.C. §103(a) as being unpatentable over Zumkehr and further in view of Keeth et al. (US 6,687,185; hereinafter, "Keeth"). Applicants respectfully traverse the rejection. Claim 6 depends from claim 1, and thus, includes every limitation set forth in claim 1. As discussed above, Zumkehr fails to disclose the limitation of a plurality of I/O buffers coupled to the plurality of DLLs to output the plurality of signals to one or more memory devices coupled to the memory interface after adjusting the timing. Further, Keeth fails to make up the deficiencies in Zumkehr. Keeth discloses a clock tree model in an output data path for setting and compensating read latency (Keeth, abstract; Figures 1 and 2). Keeth does not disclose a plurality of I/O buffers coupled to the plurality of DLLs to output the plurality of signals to one or more

memory devices coupled to the memory interface after adjusting the timing. Since neither Zumkehr nor Keeth, alone or in combination, discloses every limitation set forth in claim 6, claim 6 is patentable over Zumkehr in view of Keeth. Withdrawal of the rejection is respectfully requested.

Claims 18-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Zumkehr and further in view of Wyatt (US 6,891,543). Applicants respectfully traverse the rejection. Claim 18 sets forth:

> a plurality of input/output (I/O) buffers coupled to the plurality of DLLs to output the plurality of signals to one or more of the plurality of memory devices after adjusting the timing.

(Claim 18 as amended)

For the reason discussed above with respect to claim 1, Zumkehr fails to disclose the above limitation. Further, Wyatt does not make up the deficiencies of Zumkehr. Wyatt discloses a graphics chip and an interface engine coupled to a memory device (Wyatt, col. 9, ln. 49 – col. 10, ln. 3). Wyatt does not disclose a plurality of I/O buffers coupled to the plurality of DLLs to output the plurality of signals to one or more of the plurality of memory devices after adjusting the timing. Since neither Zumkehr nor Wyatt, alone or in combination, discloses every limitation set forth in claim 18, claim 18 is patentable over Zumkehr in view of Wyatt. Withdrawal of the rejection is respectfully requested.

Claims 19-22 depend, directly or indirectly, from claim 18. Thus, for the reason discussed above with respect to claim 18, claims 19-22 are patentable over Zumkehr in view of Wyatt. Withdrawal of the rejection is respectfully requested.

CONCLUSION

Applicants respectfully submit that the objection and rejections have been overcome by the amendments and remarks, and that the pending claims are in condition for allowance. Accordingly, Applicants respectfully request the rejections be withdrawn and the pending claims be allowed.

Pursuant to 37 C.F.R. §1.136(a)(3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. §§1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
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